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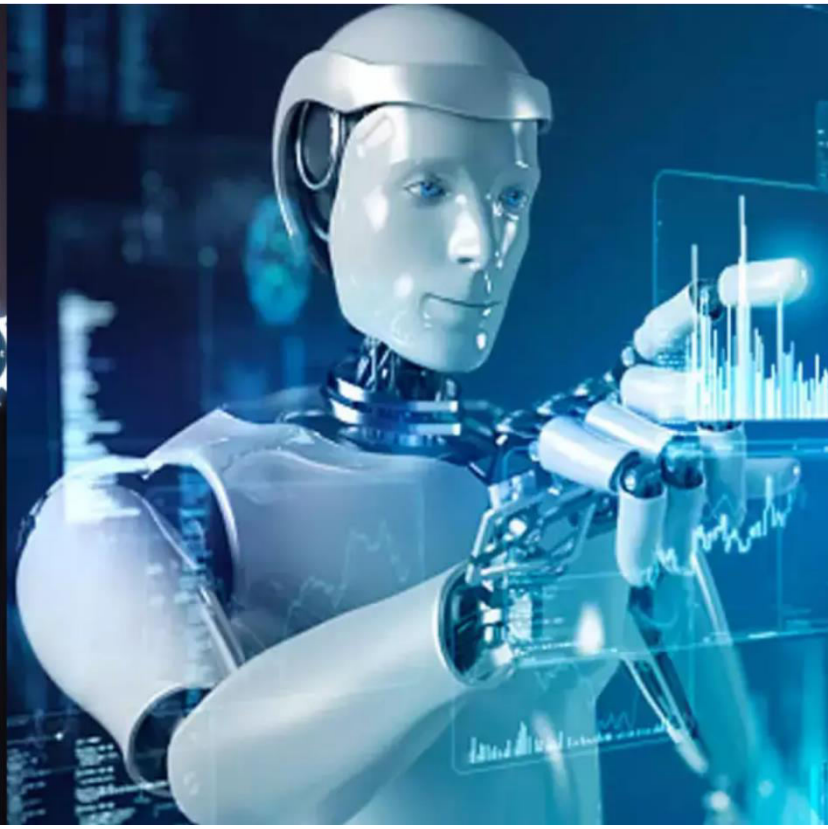

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Verilog-Based Single-Cycle RISC-V Processor with Integrated Code Converters: Design and Synthesis

Sruthi.Y[1], Lakshmi Poojitha. B[2], Yogeendra. CH[3], Siva Sai Subhaskara Rao. B[4], Jeethendra. G[5]

Professor, Department of ECE, Bapatla Engineering College, Andhra Pradesh, India[1]

Student, Department of ECE, Bapatla Engineering College, Andhra Pradesh, India[2,3,4,5]

ABSTRACT: The architecture of a RISC-V processor is essential for obtaining effective computational performance in many embedded systems. The system presented here employs a RISC-V processor with code converters to offer processing flexibility. The RISC-V processor is capable of executing basic instructions like arithmetic and logic, control operations, memory access, and conditional branching. The processor architecture incorporates program counter, instruction memory, register file, execution unit, and ALU Control Unit modules that enable the instructions to be executed in single cycle. The integration of code converters enhances the ability of the system to efficiently deal with a number of different data types. The code converters enable the processor to execute various kinds of coded data, such as binary-to-gray code conversion, gray-to-binary conversion, binary-coded decimal (BCD) conversion, and BCD-to-binary conversion. Diversity is enhanced with the use of such converters, particularly in situations requiring translation of data format, such as sensor-based applications or communication systems. Future applications in real-time systems will gain advantage from this architecture's sophisticated technique for processor design that enhances both instruction execution and data handling.

KEYWORDS: Embedded Systems, Code Converters, RISC-V Processor, Gray Code, and BCD Conversion.

I. INTRODUCTION

At its core, RISC (Reduced Instruction Set Computing) processor design focuses on extreme optimization. The philosophy is simple: single-cycle basic instructions outperform complex multi-step operations. This contrasts sharply with CISC (Complex Instruction Set Computing) architectures, where some instructions might require dozens of cycles to complete.

The RISC advantage comes from its streamlined approach. By minimizing the instruction count per program, these processors achieve two key benefits:

1. Simplified hardware design
2. Faster instruction execution

This lean methodology delivers what really matters - superior processing performance. Modern implementations take this further with techniques like:

- Advanced pipelining
- Parallel execution
- Smart branch prediction

The processor finishes basic operations such as data movement and arithmetic within a few cycles in a standard RISC architecture. It reduces memory access time by keeping temporary results in a large number of registers. Improved pipelining, parallelism, and performance optimization are achieved made

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possible by the simplicity of RISC instructions. RISC concepts are often implemented by modern processors, such as those found in smartphones, servers, and embedded systems, and accompanied with advanced methods such as branch prediction, speculative execution, and out-of-order execution. One RISC flavor that has attracted a lot of attention as it is open-source and extensible is the RISC-V architecture. Easy to learn, versatile, and easily modifiable, RISC-V is intended for use in many kinds of applications. By enabling designers to customize and add to the basic architecture according to specific needs, its open-source nature encourages innovation. This flexibility makes it possible to design unique RISC- V processors that can adapt to certain tasks or power limitations, which is crucial in the field of specialized hardware and embedded systems.

Custom RISC-V processor design enables the development of unique hardware mechanisms that satisfy the demands for modern applications. To enhance speed for specific tasks, the designers can modify the memory architecture or introduce special instructions using the open architecture of RISC-V. Due to its versatility, RISC-V is gaining momentum both in the industry and research communities, where there is a developing need for specialty computing technologies. The combination of code converters with tailored RISC-V architectures becomes a critical building block for more specialized and effective computing systems as the need for tailored computing systems grows.

II. LITERATURE SURVEY

Researchers have been actively exploring RISC-V processor implementation using Verilog, particularly focusing on pipeline optimization and advanced code conversion techniques. These investigations are paving the way for next-generation processors that balance three critical factors:

- Power efficiency
- Execution speed
- Hardware optimization

The foundation for modern RISC-V development comes from Waterman et al.'s seminal work [1], which first documented the complete RISC-V Instruction Set Architecture. This crucial reference details:

- Instruction behavior and formats
- Addressing modes
- The ISA's modular organization

What makes RISC-V particularly interesting is its compartmentalized design. The instruction set is divided into distinct subsets (integer, floating-point, atomic, and vector operations), allowing designers to mix and match extensions based on specific application needs. The specification also covers privileged mode operations - essential functionality for processors that need to support modern operating systems.

In presenting their Computer Organization and Design (RISC-V Edition), Patterson and Hennessy [2] went into a lot of details about memory hierarchy, instruction-level parallelism, processor architecture, and performance optimizations. The book discusses single-cycle, multi-cycle, and pipelined implementations of RISC-V-based processors and explains them step-by-step. It refers to performance- enhancing methods such as branch prediction, forwarding, and out-of-order execution. The authors describe the advantages of RISC-V in terms of rapid utilization, scalability, and energy efficiency by comparing it with other ISA's.

Asanović and Patterson's The RISC-V Reader [3] explains why RISC-V was created, highlighting its advantages over proprietary ISA's like x86 and ARM. The book covers instruction formats, registers, and software compatibility while analyzing design trade-offs. It also shows RISC-V's real-world uses in research, high-performance computing, and embedded systems, making it a practical guide for engineers and researchers.

A comprehensive overview of digital design and hardware description languages (Verilog, VHDL, and System Verilog) was provided by Mano and Ciletti [4]. With a focus on hardware description language (HDL) implementation, this book addresses the fundamentals of state machines, arithmetic circuits, and combinational and sequential logic design. A

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useful reference for engineers designing RISC-V processors, the book describes Verilog coding practices, synthesis boundaries, and FPGA design issues. Case studies of microprocessor and digital circuit design are included in the book.

In depth analysis of the design philosophy of the RISC-V ISA was given by Waterman and Asanovic [5], showing the flexibility, modularity, and simplicity of the ISA. The writers explain how, as compared to x86 and ARM, RISC-V was designed to be open for use. The writers examine how the modularity of instruction set and the flexible opcode encoding in RISC-V induce implementation efficiency. The research demonstrates the benefit of RISC-V's slimmed-down instruction set through a comparison of its performance and power efficiency with that of other architectures.

A strong BCD-to-binary conversion strategy for high-performance arithmetic units has been suggested by Zhang et al. [6] and is useful in mathematical calculation. The duration required and the power consumption during BCD-to-binary conversion are reduced by the authors' design-efficient approach to make it easier for integration within RISC-V processors. The research indicated that the suggested process performed faster using less hardware when compared to common conversion techniques. Nevertheless, its structure consumed more logic resources, raising the overall area usage of the processor.

With a focus on reducing dynamic power consumption and switching activity, Gupta and Kumar [7] presented a low-power binary-to-gray code converter. To minimize the number of bit transitions in Gray code conversion, the authors constructed a reduced-logic circuit. Their research is particularly related to low-power devices in which power dissipation should be minimized. Compared to conventional binary-to-Gray conversion methods, the research indicated their technology significantly cut down power consumption. But it required additional control logic, which complicated the circuit slightly.

III. CONTRIBUTION

In this article, we suggest a RISC-V(RV32I) processor design in Verilog with built-in code conversions to enhance efficiency in processing and data conversions. Our main objective is to enhance the processor's versatility through effortless data format conversion, as long as instructions are processed faultlessly in different computing environments Our design implements binary-to-Gray, Gray-to-binary, BCD-to-binary, and binary-to-BCD converters to handle multiple data formats efficiently. Synthesized using Vivado 2024.1, this FPGA-optimized approach enhances a RISC-V processor's data processing capabilities while maintaining hardware efficiency. The solution enables seamless numerical conversions with minimal performance impact.

IV. PROPOSED SYSTEM

Our RISC-V processor combines efficient instruction execution with built-in code conversion for enhanced compatibility. The five-stage pipeline (fetch, decode, execute, memory access, writeback) works alongside conversion modules to handle multiple data formats. This optimized design delivers both performance and flexibility for embedded applications.

In order to achieve a scalable and optimized solution, the design integrates various hardware modules like Program Counter, Register File, Immediate Generator, ALU and ALU Control Unit, Code Converters, Control Unit, Memory Modules, Branch Prediction and MUX . The processor is synthesized and simulated in the Vivado 2024.1, and then functionally verified prior to its deployment in hardware.

To add the code converters in RISC-V processor, the custom instructions are used which are set for user- defined extensions. Custom instructions are basically used by changing the decode and execution stages of the processor.
This system would enhance computer performance and information manipulation by utilizing the code converters, hence suitable for applications requiring other forms of number.

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4.1 Architecture Design:

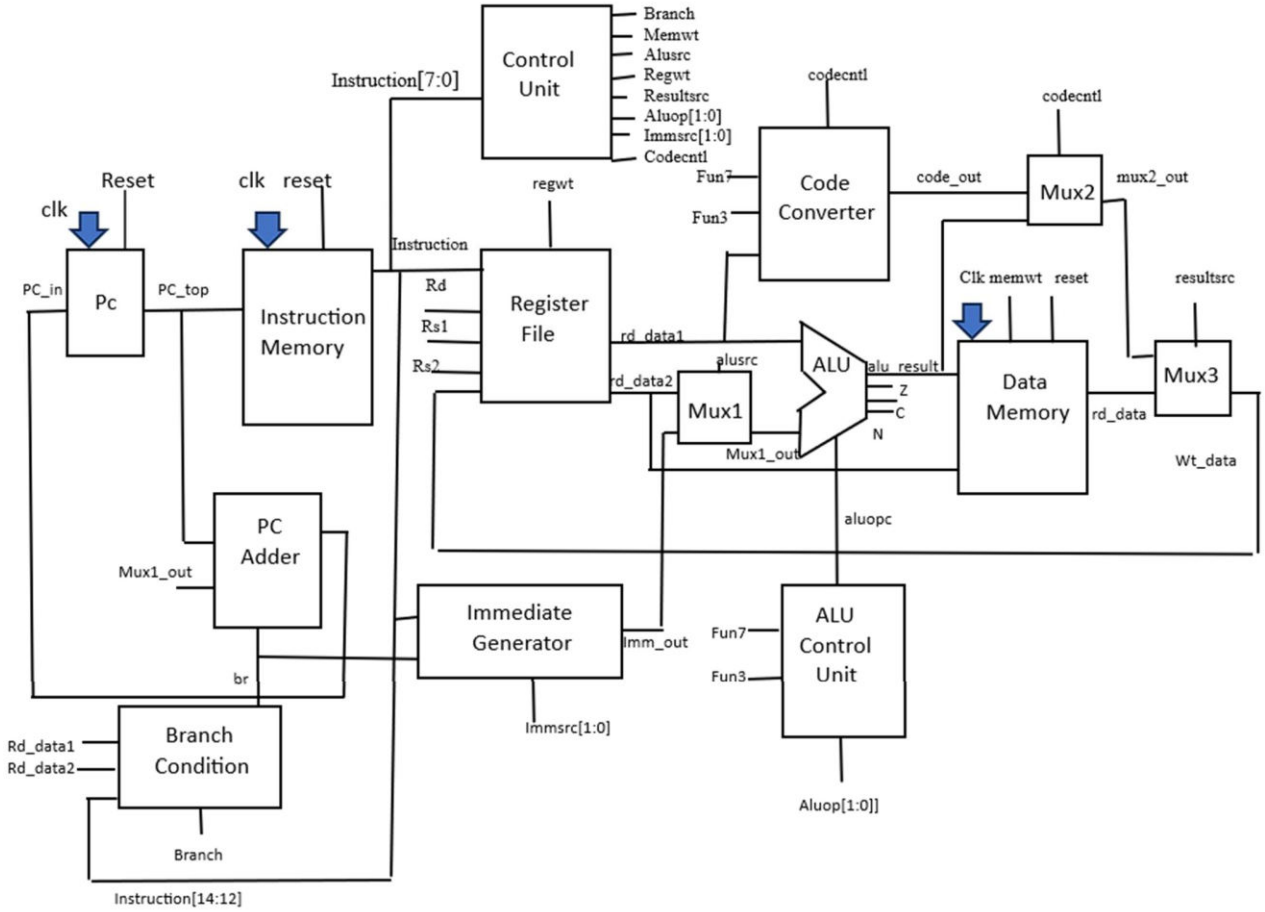

Fig.1.Block diagram of proposed method

These are the elements of the RISC-V processor that incorporates code converters: 4.1.1.Program Counter:
The location of the following instruction that needs to be loaded in order to be executed is contained in a significant register called the Program Counter (PC) of a processor.In the course of program execution, it ensures that each instruction is followed out in the correct sequence.

Instruction Memory:
Instruction memory performs the function of
storing information and providing the instructions that the processor must execute. It contains the machine code of the programs, which the processor receives, decodes, and executes.

Register File:
A Register File is a group of registers employed to store addresses, control data, and temporary information. The processor's fastest memory components, these registers are employed to reduce its reliance on main memory and accelerate data access.

Immediate Generator:
One basic building block of the instruction decoding process of a processor is an Immediate Generator (Imm Gen). It performs the immediate value extraction, sign expansion, and instruction code structuring

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ALU Unit (ALU and ALU Control Unit):
Part of the core requirements of a processor is the Arithmetic Logic Unit, or ALU. It carries out all the bitwise, logical, and arithmetic functions necessary to execute instructions. Together with ALU Control Unit making it able to work in a efficiently in a is collectively called the ALU Unit.
ALU Control Unit assists the ALU in determining which operations to be executed according to the base RISC-V opcodes and function fields in the instruction being executed.

Code Converters:
The system implements code converters to enable seamless data translation between different binary formats, ensuring compatibility across devices with varying encoding schemes. Gray code proves particularly valuable for digital logic with its single-bit transition property between consecutive values, while BCD's 4-bit per digit representation simplifies decimal-binary conversions. These converters are integrated into the processor using a custom 0 opcode for efficient hardware implementation.

Data Memory:
The data memory stores and accumulates the data that the processor needs to perform operations. Because it stores information such as variables, instructions, and execution-dependent intermediate results, it is a critical element of the processor's design. Instruction memory, which stores the executable instructions of the program, is generally distinct from data memory.

Branch Condition:
Branch prediction boosts processor performance by anticipating conditional branch outcomes (if-else, loops, jumps) before they're resolved. This smart optimization reduces pipeline stalls and prevents control hazards, keeping instruction flow smooth and efficient.

Control Unit:
The control unit serves as the brain of the RISC-V processor, decoding instruction opcodes and generating the necessary control signals to coordinate operations across the ALU, register file, and memory. It determines execution flow by analysing each instruction and precisely timing signal delivery to all CPU components.

MUX:
A MUX (Multiplexer) is a critical processor and digital circuit component that manages data routing. A multiplexer, a combinational logic circuit, can select one of several input signals and forward the selected input to a single output line. It is commonly utilized in communication circuits, memory systems, and processors to better manage multiple data inputs.

Here we have utilized 3 multiplexers to choose the needed input as the output.

4.2 Software :

A Complete Development Environment: Xilinx Vivado Design Suite

A robust FPGA development environment for designing, modelling, synthesizing, and implementing digital circuits is the Xilinx Vivado Design Suite.

Xilinx's Vivado is a fantastic choice for beginner and advanced engineers alike due to its intuitive interface and extensive set of hardware description language (HDL) tools.

Vivado's Tcl-based and graphical process, enabling users to efficiently design and optimize FPGA-based projects, is one of its primary strengths. Vivado simplifies the process of converting HDL designs into bit streams that can be programmed onto Xilinx FPGA devices with its built-in synthesis, simulation, and debugging tools.

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Vivado offers several new features that enhance FPGA development and digital design:

1. Graphical User Interface.
2. Support for High-Level Languages.
3. Integrated Cores and Libraries for IP.
4. Complete Simulation and Debugging.
5. Optimized Synthesis and Implementation for FPGA.
6. Power Analysis and Optimization.

Therefore, Vivado 2024.1 was utilized to synthesize the Register Transfer Level (RTL) design that was developed through the use of Verilog.

V. SIMULATION AND ANALYSIS

The simulation of the top-level module of the RISC-V processor design demonstrates that the processor fetches, decodes, executes, and writes back instructions in a single clock cycle in a correct manner. It properly manages branch conditions and memory operations so that RISC-V programs execute correctly and efficiently.

VI. CONCLUSION

Significant advancements in flexibility and scalability are offered by the proposed RISC-V processor incorporating code converters within it, making it relevant to several computing applications. The successful synthesis of the design attests that the design can be realized in the real world. Code converters enhance the usability of the processor in embedded and high-performance computing domains by enhancing flexibility with diverse data formats. In order to further enhance the performance of the processor, future research will focus on the pipeline design, and power efficiency.

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